

ABSTRACT OF THE DISCLOSURE

An adder for adding a signal at a first input (A) and a second input (B) to produce an adder output (S) is disclosed. The adder comprises a bypass input (bypass) and a logic circuit, communicatively coupled to the bypass input (bypass), the first input (A), and the second input (B), the logic circuit configured to hold at least one of the first input (A) and the second input (B) according to the bypass input (bypass).

*Express Mail® mailing label number EL815953549US
Date of Deposit August 24 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to:
Commissioner for Patents, Washington, D.C. 20231.

Adriane M Baird
(Printed Name)

Adriane M Baird
(Signature)